**Lab 1: Introduction to Quartus II Software Design**

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**Lab Problem:**

During the lab we will be making a simple logic circuit for a circuit with AND, NAND and NOR gates. Through the objectives marked below, this lab is very important to initiate students with no background with Altera Quartus II. This lab is also very important as a reminder to the software for the students who have already used Altera Quartus.

**Objectives:**

* To initiate the students who are not familiar with the Altera Quartus II Software Design
* To act as a review for the more advance students.
* Understand the basic of the Altera environment.
* Design a simple logic circuit using the Graphic editor.
* Compile, simulate, debug, and test their design.
* Download and run their design on the Altera DE2-115 board.

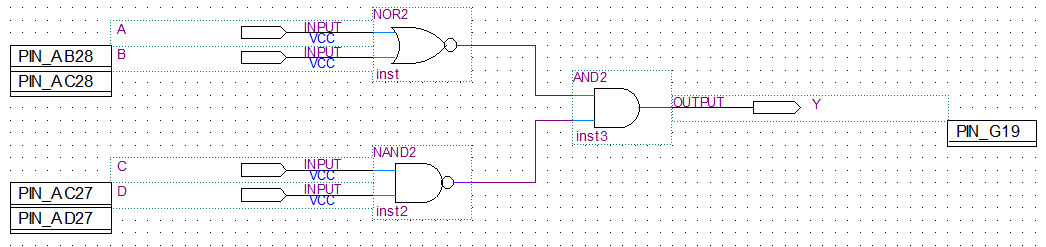
**Solution:**

To find the solution, we first made a boolean equation ((A+B)’(CD)’) from the circuit given to us. From that equation we made 2 truth tables for each section leading to the AND. From the 2 truth tables we derived the final truth table. (Check Appendix figure 3 for pre-lab)

**Materials:**

* Quartus II 13.0 Service-Pack 1 Program
* Altera DE2-115 card

**Design:**



**Figure 1: Screen Capture of simple circuit with AND, NAND and NOR gates Schema**

**Equation:** (A+B)’(CD)’ = Y

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **D** | **Y** |
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 |

**Table 1 : Experimental Data Observed from the Altera DE2-115 Card Circuit**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **AB\CD** | **00** | **01** | **11** | **10** |
| **00** | 1 | 1 | 0 | 1 |
| **01** | 0 | 0 | 0 | 0 |
| **11** | 0 | 0 | 0 | 0 |
| **10** | 0 | 0 | 0 | 0 |

**Table 2 : Karnaugh Map of Experimental Data Observed from the Altera DE2-115 Card Circuit**

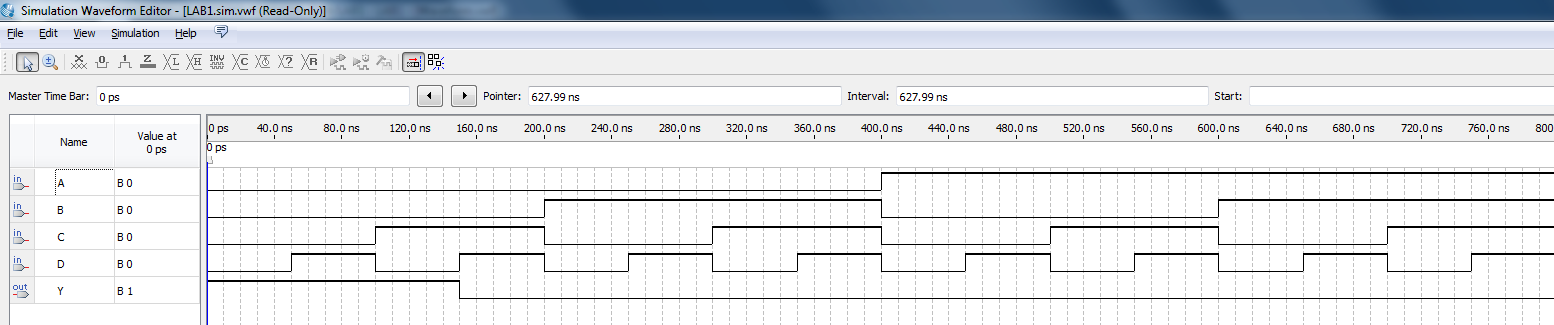
**Discussion of used Components:** The circuit contains AND, NAND and NOR gates. The AND gate returns 1 if both inputs are 1. The NAND gate returns 1 if none or 1 of the inputs are 1. Finally the NOR gate returns 1 if both inputs are 0. (A, B going into NOR and C, D going into NAND )

**Discussion of Actual Solution:** With all the components working together, the NAND and NOR gate leading to the AND gate, the output should only be 1 if A, B are 0 and C, D any combination excluding 1, 1. We used the simulation to test our truth table (explained below), and we were able to conclude that our design and derived truth table was correct.

**Discussion of Tool:** The tools we used were the Quartus II software and card. During the simulation process we were able to determine if we had derived a correct truth table. In the simulation (figure 2). Every 1 and 0 are indicated by the bumps up and down. With this method we were able to see that our pre-lab was correct.

**Discussion of Challenging Problems:** A very challenging problem we faced during the laboratory was the “Device Manager” we could not figure out how to get the logic gates into the list. It proved to be a simple solution, we had forgotten to compile a second time.

**Simulation and Verification:**

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**Figure 2 : Simulation of simple circuit with AND, NAND and NOR gates**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **D** | **Theoretical Output**  **Y** | **Experimental Output Y** |
| 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 |

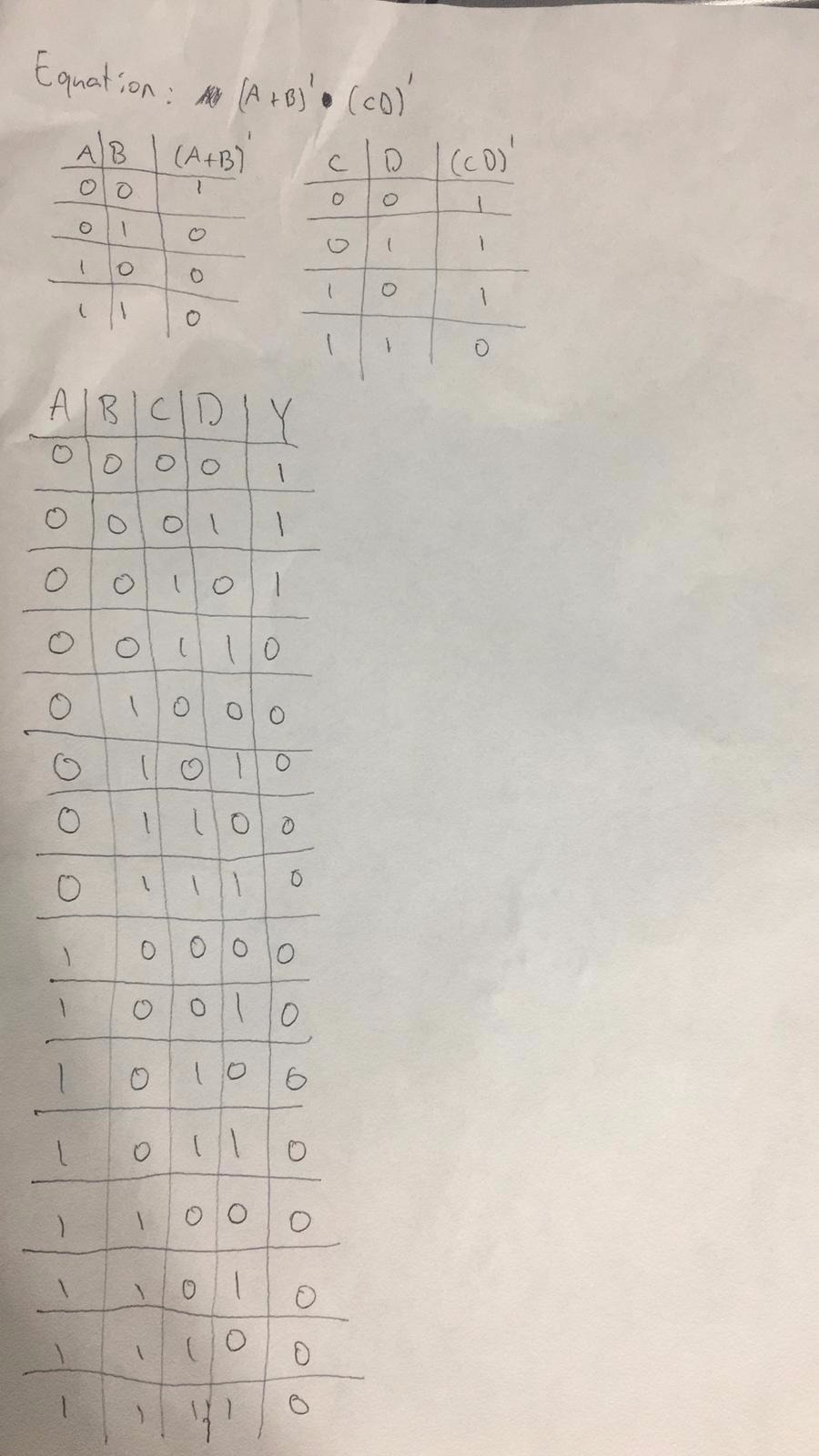
**Table 1 : Theoretical Data vs. Experimental Data Observed from the Altera DE2-115 Card Circuit**

**Experimental verification of Operation of the Circuit:** As seen above, our theoretical data was a match to the experimental data, achieved by loading our circuit onto the Altera board and testing each combination, meaning that our design was correct and the outcome expected. Our simulation followed a path that was described in our pre-lab.

**Conclusion:**

This lab did not contain any problems for us and the results given at the end were exactly what we predicted. The simple circuit with AND, NAND and NOR gates had an output of 1 if A, B were both 0, and C, D were any combination except for 1 and 1. To prove that such was the case, a simulation was ran (were the outcome was what we predicted), and an Altera Card was loaded with the circuit, and tested (again with expected results). At the end of the lab, we were able to get comfortable with the software and were able to replicate the circuit.

**Appendix:**



**Figure 3: Pre-lab**